Data Sheet for Serial FPDP IP Core
# Table of Contents

1. GENERAL DESCRIPTION ......................................................... 5  
2. FEATURES ........................................................................ 5  
3. BLOCK DIAGRAM ................................................................. 6  
4. IO SIGNALS ......................................................................... 7  
5. FUNCTIONAL DESCRIPTION .................................................. 9  
6. TIMING WAVEFORMS ......................................................... 10  
7. RESOURCE UTILIZATION .................................................... 12
List Of Figures

Figure 1: Serial FPDP IP Core Block Diagram ............................................................. 6
Figure 2: Unframed Data ......................................................................................... 10
Figure 3: SUSPEND Timing .................................................................................... 10
Figure 4: Single Frame Data .................................................................................. 10
Figure 5: Repeating Frame Data ........................................................................... 11
List Of Tables

Table 1: Serial FPDP IP Core IO Signals ................................................................. 7
Table 2: Device Utilization Summary for Xilinx Virtex-5 ........................................ 12
Table 3: Device Utilization Summary for Altera Stratix IV ..................................... 12
Table 4: Device Utilization Summary for Lattice ECP3 ............................................ 12
1. General Description

The ANSI/VITA 17.1-2003, or Serial Front Panel Data Port (FPDP), standard provides a relatively simple protocol for point-to-point data links between a sensor and a processor, using more than 99 percent of the available throughput with a minimum of protocol overhead. In addition to link efficiency, the simplicity of the protocol makes it easy to implement a Serial FPDP endpoint in an FPGA. The Serial FPDP standard supports three data rates: 1.0625 Gbaud, 2.125 Gbaud, and 2.500 Gbaud. Control and data packets are encoded using 8B/10B encoding, resulting in data transfers at 247 megabytes per second using a 2.5 GBd serial link after encoding and protocol overhead. Serial FPDP links support a wide range of physical interfaces with the most common option being 2.5 gigabits per second multimode fiber.
iWave Serial Front Panel Data Port (sFPDP) IP core for FPGA is based on the ANSI/VITA 17.1-2003 standard. This intellectual property core can be implemented on any transceiver based Xilinx/Altera/Lattice FPGAs.

2. Features

The following are the main features of the Serial FPDP IP core:

- Compliant with ANSI/VITA 17.1-2003 Serial FPDP standard
- Supported link speeds
  - 1.0625 Gbaud
  - 2.125 Gbaud
  - 2.5 Gbaud
- Data Frames supported
  - Unframed Data
  - Single Frame Data
  - Fixed Size Repeating Frame Data
  - Dynamic Size Repeating Frame Data
- System Configurations supported
  - Basic System
  - Flow Control
  - Bi-directional Data Flow
  - Copy Mode
  - Copy/Loop Mode
- Host-Bus interface
  - Parallel FPDP
- Configurable parameters
  - Transmit FIFO depth
  - Receive FIFO depth
  - Transmit FIFO watermark to assert SUSPEND output
  - Receive FIFO watermark for STOP/GO signal generation
  - Transceiver Interface Data Width
3. Block Diagram

![Serial FPDP IP Core Block Diagram](image)

Figure 1: Serial FPDP IP Core Block Diagram
## 4. IO Signals

### Table 1: Serial FPDP IP Core IO Signals

<table>
<thead>
<tr>
<th>Signal</th>
<th>Dir</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Clock &amp; Reset Signals</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>rst_n_i</td>
<td>I</td>
<td>1</td>
<td>Reset</td>
</tr>
<tr>
<td>fpdp_clk_i</td>
<td>I</td>
<td>1</td>
<td>FPDP Clock</td>
</tr>
<tr>
<td>sfpdp_clk_i</td>
<td>I</td>
<td>1</td>
<td>sFPDP Clock</td>
</tr>
<tr>
<td><strong>Control &amp; Status Signals</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>en_tx_i</td>
<td>I</td>
<td>1</td>
<td>Transmitter Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When HIGH enables transmission of sFPDP frames.</td>
</tr>
<tr>
<td>en_rx_i</td>
<td>I</td>
<td>1</td>
<td>Receiver Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When HIGH enables receiving of sFPDP frames.</td>
</tr>
<tr>
<td>en_flowcontrol_i</td>
<td>I</td>
<td>1</td>
<td>Flow Control Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When HIGH enables flow</td>
</tr>
<tr>
<td>en_copymode_i</td>
<td>I</td>
<td>1</td>
<td>Copy Mode Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When HIGH enables copy mode of operation.</td>
</tr>
<tr>
<td>en_tx_crc_i</td>
<td>I</td>
<td>1</td>
<td>Transmitter CRC enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When HIGH enables generation of CRC in transmit sFPDP frames.</td>
</tr>
<tr>
<td>en_rx_crc_i</td>
<td>I</td>
<td>1</td>
<td>Receiver CRC enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When HIGH enables checking of CRC in receive sFPDP frames.</td>
</tr>
<tr>
<td>rx_crc_error_o</td>
<td>O</td>
<td>1</td>
<td>Receive CRC Error</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When HIGH indicates sFPDP frame received with CRC error.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Signal driven from sfpdp_clk domain.</td>
</tr>
<tr>
<td>remote_txfifo_ovr_o</td>
<td>O</td>
<td>1</td>
<td>Remote Transmit FIFO Overflow</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When HIGH indicates Transmit FIFO Overflow received from remote transmitter.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Signal driven from sfpdp_clk domain.</td>
</tr>
<tr>
<td><strong>FPDP Signals</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fpdp_rx_d_i</td>
<td>I</td>
<td>32</td>
<td>D[31:0] from FPDP</td>
</tr>
<tr>
<td>Signal</td>
<td>Dir</td>
<td>Width</td>
<td>Description</td>
</tr>
<tr>
<td>-------------------</td>
<td>-----</td>
<td>-------</td>
<td>---------------------------</td>
</tr>
<tr>
<td>fpdp_rx_dir_n_i</td>
<td>I</td>
<td>1</td>
<td>DIR* from FPDP</td>
</tr>
<tr>
<td>fpdp_rx_sync_n_i</td>
<td>I</td>
<td>1</td>
<td>SYNC* from FPDP</td>
</tr>
<tr>
<td>fpdp_rx_dvalid_n_i</td>
<td>I</td>
<td>1</td>
<td>DVALID* from FPDP</td>
</tr>
<tr>
<td>fpdp_rx_pio1_i</td>
<td>I</td>
<td>1</td>
<td>PIO1 from FPDP</td>
</tr>
<tr>
<td>fpdp_rx_pio2_i</td>
<td>I</td>
<td>1</td>
<td>PIO2 from FPDP</td>
</tr>
<tr>
<td>fpdp_rx_nrdy_n_o</td>
<td>O</td>
<td>1</td>
<td>NRDY* to FPDP</td>
</tr>
<tr>
<td>fpdp_rx_suspend_n_o</td>
<td>O</td>
<td>1</td>
<td>SUSPEND* to FPDP</td>
</tr>
<tr>
<td>fpdp_tx_d_o</td>
<td>O</td>
<td>32</td>
<td>D[31:0] to FPDP</td>
</tr>
<tr>
<td>fpdp_tx_dir_n_o</td>
<td>O</td>
<td>1</td>
<td>DIR* to FPDP</td>
</tr>
<tr>
<td>fpdp_tx_sync_n_o</td>
<td>O</td>
<td>1</td>
<td>SYNC* to FPDP</td>
</tr>
<tr>
<td>fpdp_tx_dvalid_n_o</td>
<td>O</td>
<td>1</td>
<td>DVALID* to FPDP</td>
</tr>
<tr>
<td>fpdp_tx_pio1_o</td>
<td>O</td>
<td>1</td>
<td>PIO1 to FPDP</td>
</tr>
<tr>
<td>fpdp_tx_pio2_o</td>
<td>O</td>
<td>1</td>
<td>PIO2 to FPDP</td>
</tr>
<tr>
<td>fpdp_tx_nrdy_n_i</td>
<td>I</td>
<td>1</td>
<td>NRDY* from FPDP</td>
</tr>
<tr>
<td>fpdp_tx_suspend_n_i</td>
<td>I</td>
<td>1</td>
<td>SUSPEND* from FPDP</td>
</tr>
</tbody>
</table>

**Transceiver Signals**

<table>
<thead>
<tr>
<th>Signal</th>
<th>Dir</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>sfpdp_tx_data_o</td>
<td>O</td>
<td>32</td>
<td>Transmit Data</td>
</tr>
<tr>
<td>sfpdp_tx_datak_o</td>
<td>O</td>
<td>4</td>
<td>Transmit Control Enable</td>
</tr>
<tr>
<td>sfpdp_rx_data_i</td>
<td>I</td>
<td>32</td>
<td>Receive Data</td>
</tr>
<tr>
<td>sfpdp_rx_datak_i</td>
<td>I</td>
<td>4</td>
<td>Receive Control Enable</td>
</tr>
</tbody>
</table>
5. Functional Description

The main blocks in Serial FPDP IP core are:

- **Transmitter**: On the transmit side, the parallel FPDP data is converted to Serial FPDP. It consist of mainly 3 modules.
  - **FPDP In**: Used to receive data from host bus (FPDP bus).
  - **FIFO**: Used to store the data from FPDP data frame.
  - **Framer**: Used to frame sFPDP data frames and send to transceiver.
- **Receiver**: On the receive side, the Serial FPDP data is converted back into the FPDP parallel data stream. It consist of mainly 3 modules.
  - **Deframer**: Used to deframe the data frames coming for sFPDP link.
  - **FIFO**: Used to store the data from decoded sFPDP data frame.
  - **FPDP Out**: Used to drive the data to host-bus using FPDP bus.
6. Timing Waveforms

Below waveforms shows the timing diagram of Host-Bus interface

Figure 2: Unframed Data

Figure 3: SUSPEND Timing

Figure 4: Single Frame Data
Figure 5: Repeating Frame Data
7. Resource Utilization

The table below shows the utilization summary from the implementation of Serial FPDP IP core for different FPGA devices. IP configured for following

1. Tx FIFO depth 1024
2. Rx FIFO depth 1024
3. Transceiver interface data width 32-bit

Table 2: Device Utilization Summary for Xilinx Spartan-6 LXT

<table>
<thead>
<tr>
<th>Logic Utilization</th>
<th>Used</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slice Registers</td>
<td>592</td>
</tr>
<tr>
<td>Slice LUTs</td>
<td>803</td>
</tr>
<tr>
<td>RAMB16BWERs</td>
<td>4</td>
</tr>
</tbody>
</table>

Table 3: Device Utilization Summary for Xilinx Virtex-5 LXT

<table>
<thead>
<tr>
<th>Logic Utilization</th>
<th>Used</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slice Registers</td>
<td>592</td>
</tr>
<tr>
<td>Slice LUTs</td>
<td>809</td>
</tr>
<tr>
<td>36K Block RAMs</td>
<td>2</td>
</tr>
</tbody>
</table>

Table 4: Device Utilization Summary for Altera Cyclone IV GX

<table>
<thead>
<tr>
<th>Logic Utilization</th>
<th>Used</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic Cells</td>
<td>970</td>
</tr>
<tr>
<td>Dedicated Logic Registers</td>
<td>496</td>
</tr>
<tr>
<td>M9Ks</td>
<td>9</td>
</tr>
</tbody>
</table>

Table 5: Device Utilization Summary for Altera Stratix IV GX

<table>
<thead>
<tr>
<th>Logic Utilization</th>
<th>Used</th>
</tr>
</thead>
<tbody>
<tr>
<td>Combinational ALUTs</td>
<td>717</td>
</tr>
<tr>
<td>Dedicated Logic Registers</td>
<td>497</td>
</tr>
<tr>
<td>M9Ks</td>
<td>9</td>
</tr>
</tbody>
</table>

Table 6: Device Utilization Summary for Lattice ECP3

<table>
<thead>
<tr>
<th>Logic Utilization</th>
<th>Used</th>
</tr>
</thead>
<tbody>
<tr>
<td>LUT4s</td>
<td>1020</td>
</tr>
<tr>
<td>Registers</td>
<td>602</td>
</tr>
<tr>
<td>Block RAMs</td>
<td>4</td>
</tr>
</tbody>
</table>