Data Sheet for 8254 Programmable Interval Timer

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**DOCUMENT REVISION HISTORY**

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<td>VC</td>
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1 Introduction

1.1 Purpose
This document describes the Technical Specification 8254 programmable interval timer. It includes the overall features, detailed description, I/O specifications and resource utilization summary for the 8254 programmable interval timer.

1.2 Features
Following are the 8254 Programmable interval timer features
- Three independently operated 16-bit counters
- Binary/BCD count operation
- Multiple Latch command for easy monitoring
- Counter Latch command
- Six count modes available for each counter
  - Interrupt at the End of Count
  - GATE Re-triggerable One-Shot
  - Rate Generator
  - Square Wave Generator
  - Software-Triggered Strobe
  - Re-triggerable Hardware-Triggered Strobe
- Functionally based on 8254

1.3 Acronyms and Abbreviations
Table 1: Acronyms & Abbreviations

<table>
<thead>
<tr>
<th>Term</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>BCD</td>
<td>Binary Coded Decimal</td>
</tr>
</tbody>
</table>
2 Programmable Interval Timer

2.1 Block Diagram

![Programmable Interval Timer Block Diagram]

**Figure 1:** Programmable Interval Timer Block Diagram

2.2 Description

The design implements 8254 Programmable Interval Timer/Counter used for timing control applications in microcomputer systems.

Design is capable of generating accurate time delays under software control. Three independent 16-bit counters are supported which can be configured to operate in one of the six operating modes supported.
- **Data Bus Buffer**: This is a 8-bit, three-state buffer that interfaces the system bus to the remaining blocks of the design.
- **Read/Write Control**: This block decodes the control and address inputs from the processor and generates control signals to the remaining blocks of the design.
- **Control Word Register**: This is a 8-bit register into which the control words are written to determine the operation mode of the counter.
- **Counter #n (n=0, 1, 2)**: Three independent counters capable of binary or BCD operation are supported. Each counter supports six different modes configurable through software and can each be set to different operating modes.


### 2.3 Signal Description

**Table 2: Programmable Timer IO Signal description**

<table>
<thead>
<tr>
<th>SIGNAL NAME</th>
<th>I/O</th>
<th>WIDTH</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>RESET</td>
<td>I</td>
<td>1</td>
<td>Input reset signal</td>
</tr>
<tr>
<td>D_I [7:0]</td>
<td>I</td>
<td>8</td>
<td>8-bit input data bus</td>
</tr>
<tr>
<td>D_O [7 :0]</td>
<td>O</td>
<td>8</td>
<td>8 bit output data bus</td>
</tr>
<tr>
<td>D_VAL_O</td>
<td>O</td>
<td>1</td>
<td>Output data valid signal</td>
</tr>
<tr>
<td>A [1 :0]</td>
<td>I</td>
<td>2</td>
<td>16-bit bidirectional data lines</td>
</tr>
<tr>
<td>CS_N</td>
<td>I</td>
<td>1</td>
<td>Active low Chip select input</td>
</tr>
<tr>
<td>IOWR_N</td>
<td>I</td>
<td>1</td>
<td>Active low Write enable input</td>
</tr>
<tr>
<td>IORD_N</td>
<td>I</td>
<td>1</td>
<td>Active low Read enable input</td>
</tr>
<tr>
<td>CLK0</td>
<td>I</td>
<td>1</td>
<td>Determines the count rate for Counter-0</td>
</tr>
<tr>
<td>GATE0</td>
<td>I</td>
<td>1</td>
<td>This signal controls the operation of Counter-0 depending on the mode of operation</td>
</tr>
<tr>
<td>OUT0</td>
<td>O</td>
<td>1</td>
<td>Counter-0 output, operation depends on the count mode. Can be used as an interrupt source for the processor.</td>
</tr>
<tr>
<td>CLK1</td>
<td>I</td>
<td>1</td>
<td>Determines the count rate for Counter-1</td>
</tr>
<tr>
<td>GATE1</td>
<td>I</td>
<td>1</td>
<td>This signal controls the operation of Counter-1 depending on the mode of operation</td>
</tr>
<tr>
<td>OUT1</td>
<td>O</td>
<td>1</td>
<td>Counter-1 output, operation depends on the count mode. Can be used as an interrupt source for the processor.</td>
</tr>
<tr>
<td>CLK2</td>
<td>I</td>
<td>1</td>
<td>Determines the count rate for Counter-2</td>
</tr>
<tr>
<td>GATE2</td>
<td>I</td>
<td>1</td>
<td>This signal controls the operation of Counter-2 depending on the mode of operation</td>
</tr>
<tr>
<td>OUT2</td>
<td>O</td>
<td>1</td>
<td>Counter-2 output, operation depends on the count mode. Can be used as an interrupt source for the processor.</td>
</tr>
</tbody>
</table>
3 Timing Waveforms

3.1 Count Write Operation (Ex. Mode 0)

Figure 2: Mode 0 Operation
3.2 Mode 0 Operation

![Mode 0 Operation Diagram]

Figure 3: Mode 0 Operation
3.3 Mode 1 Operation

![Diagram of Mode 1 Operation]

Figure 4: Mode 1 Operation
3.4 Mode 2 Operation

Figure 5: Mode 2 Operation
3.5 Mode 3 Operation

Figure 6: Mode 3 Operation
3.6 Mode 4 Operation

Figure 7: Mode 4 Operation
3.7 Mode 5 Operation

Figure 8: Mode 5 Operation