Data Sheet for PCIe to SD/eMMC Bridge

DOCUMENT REVISION HISTORY

Revision	Date	Change Description	Author
1.0	07th Sept'12	Internal review feedback updated	VC

Table of Contents

List Of Figures

List Of Tables

1 Introduction

1.1 Purpose

This document describes the Technical Specification of PCIe to SD/eMMC Host Bridge. It includes the overall architectural description, detailed functional specifications and interface definitions for the PCIe to SD/eMMC Host Bridge.

1.2 Features

The following are the main features of the PCIe to SD/eMMC Bridge:

- Compliant with SD Host Controller Standard Specification Version 2.0
- Compliant with SD Physical Layer Specification Version 2.0
- Compliant with eMMC Specification Version 4.41
- Supports 1-bit,4-bit SD/eMMC modes and 8-bit eMMC modes.
- Supports SD Card Detection input pin
- Supports SD Card Write Protection input pin
- Supports programmable clock frequency generation to the SD/eMMC card.
- Supports Interrupt and ADMA2 transfer mode of operation.
- Individual 2Kbyte data buffer for read and write.
- Cyclic Redundancy Check (CRC) for command and data.
- Supports timeout monitoring for response, data, CRC token & busy.
- Supports a maximum block length of 2K-byte.
- Supports both single block and multi block data transfer.
- Supports power ON/OFF control to SD/eMMC card.

1.3 Acronyms and Abbreviations

Table 1: Acronyms & Abbreviations

Term	Meaning
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
FPGA	Field Programmable Gate Array
SD	Secure Digital Card
MMC	Multi Media Card
PCIe	PCI Express

2 PCIe to SD/eMMC Bridge

2.1 Block Diagram

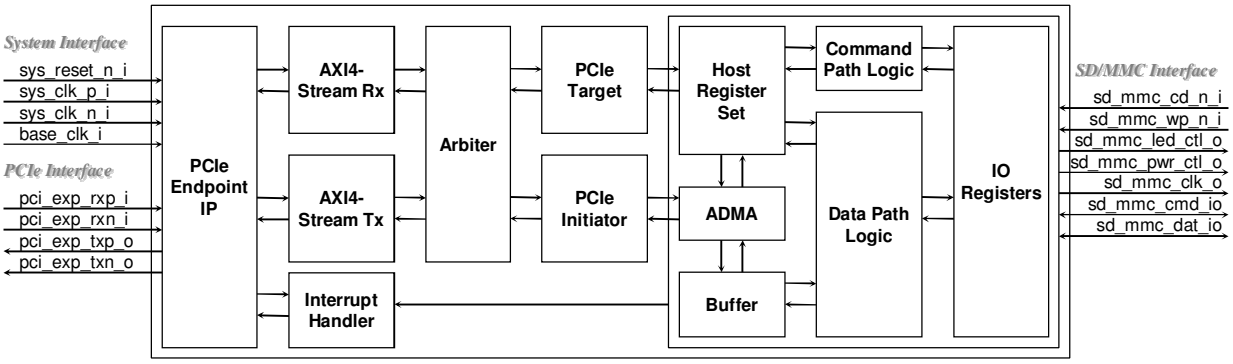

Figure 1: PCIe to SD/eMMC Bridge Block Diagram

2.2 Description

The main blocks of PCIe to SD/eMMC IP FPGA Logic are given below.

- **PCIe Endpoint**: This is a hard macro IP from Xilinx/Altera. It implements Gen1 x1 PCIe endpoint.
- **AXI4-Stream Rx**: This modules implement the AXI4-ST receive port. The AXI4-Stream receive port converts the AXI-Stream interface of the IP core to the descriptor/data interface used by the application logic.
- **AXI4-Stream Tx**: This module implement the AXI4-Stream transmit port. The AXI4-Stream transmit port converts the descriptor/data interface of the application logic to the AXI4-Stream interface of the IP core.
- **Arbiter**: This module implements arbitration logic for Tx Descriptor/Data port. Higher priority is given for completion.
- **Interrupt Handler**: Accepts interrupt from SD/eMMC host controllers and generates MSI request to PCIe IP.
- **PCIe Target**: This module provides the completer function for all downstream accesses. processes all downstream read and write requests and handles transmission of completions. Only single DWORD access is supported.
- **PCIe Initiator**: .This module generates read and write request to IP for DMA transfers.
- **Host Register Set**: This module implements standard SD host register set.
- **ADMA**: This module implements scatter gather DMA controller to transfer data from/to host memory.

- **Buffer**: Implements 2K-byte of FIFO on each read and write direction.
- **Command Path Logic**: This module implements logic required for sending command and receiving response from card.
- **Data Path Logic**: This module implements logic required for sending and receiving data from card.
- **IO Register**: This module implements input & output registers for MMC command & data lines.

2.3 IO Signals

Table 2: System Interface IO Signals

Signal	Dir	Width	Description
sys_reset_n_i	I	1	Asynchronous reset
sys_clk_p_i	I	1	Reference clock Positive
sys_clk_n_i	I	1	Reference clock Negative
base_clk_i	I	1	SD/MMC base clock

Table 3: PCIe Interface IO Signals

Signal	Dir	Width	Description
pci_exp_txp_o	O	1	PCI Express Transmit Positive: Serial Differential Output 0 (+)
pci_exp_txn_o	O	1	PCI Express Transmit Negative: Serial Differential Output 0 (–)
pci_exp_rxp_i	I	1	PCI Express Receive Positive: Serial Differential Input 0 (+)
pci_exp_rxn_i	I	1	PCI Express Receive Negative: Serial Differential Input 0 (-)

Table 4: SD/eMMC Interface IO Signals

Signal	Dir	Width	Description
sd_mmc_cd_n_i	I	1	Card Detect 0 – card present 1 – no card present

Signal	Dir	Width	Description
sd_mmc_wp_n_i	I	1	Write Protect 0 – write enabled 1 – write protected
sd_mmc_led_ctl_o	O	1	LED Control 0 – LED OFF 1 – LED ON
sd_mmc_pwr_ctl_o	O	1	Power Control 0 – Power OFF 1 – Power ON
sd_mmc_clk_o	O	1	Clock
sd_mmc_cmd_io	IO	1	Command Line
sd_mmc_dat_io	IO	8	Data Line