

# **Data Sheet For 8254 Programmable Interval Timer**

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## DOCUMENT REVISION HISTORY

Revision	Date	Change Description	Author
1.0	24th Dec '11	Initial Version	KA
REL 1.0	16th Aug '12	Removed implementation results	VC

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# 1 Introduction

## 1.1 Purpose

This document describes the Technical Specification 8254 programmable interval timer. It includes the overall features, detailed description, I/O specifications and resource utilization summary for the 8254 programmable interval timer.

## 1.2 Features

Following are the 8254 Programmable interval timer features

- Three independently operated 16-bit counters
- Binary/BCD count operation
- Multiple Latch command for easy monitoring
- Counter Latch command
- Six count modes available for each counter
  - Interrupt at the End of Count
  - GATE Re-triggerable One-Shot
  - Rate Generator
  - Square Wave Generator
  - Software-Triggered Strobe
  - Re-triggerable Hardware-Triggered Strobe
- Functionally based on 8254

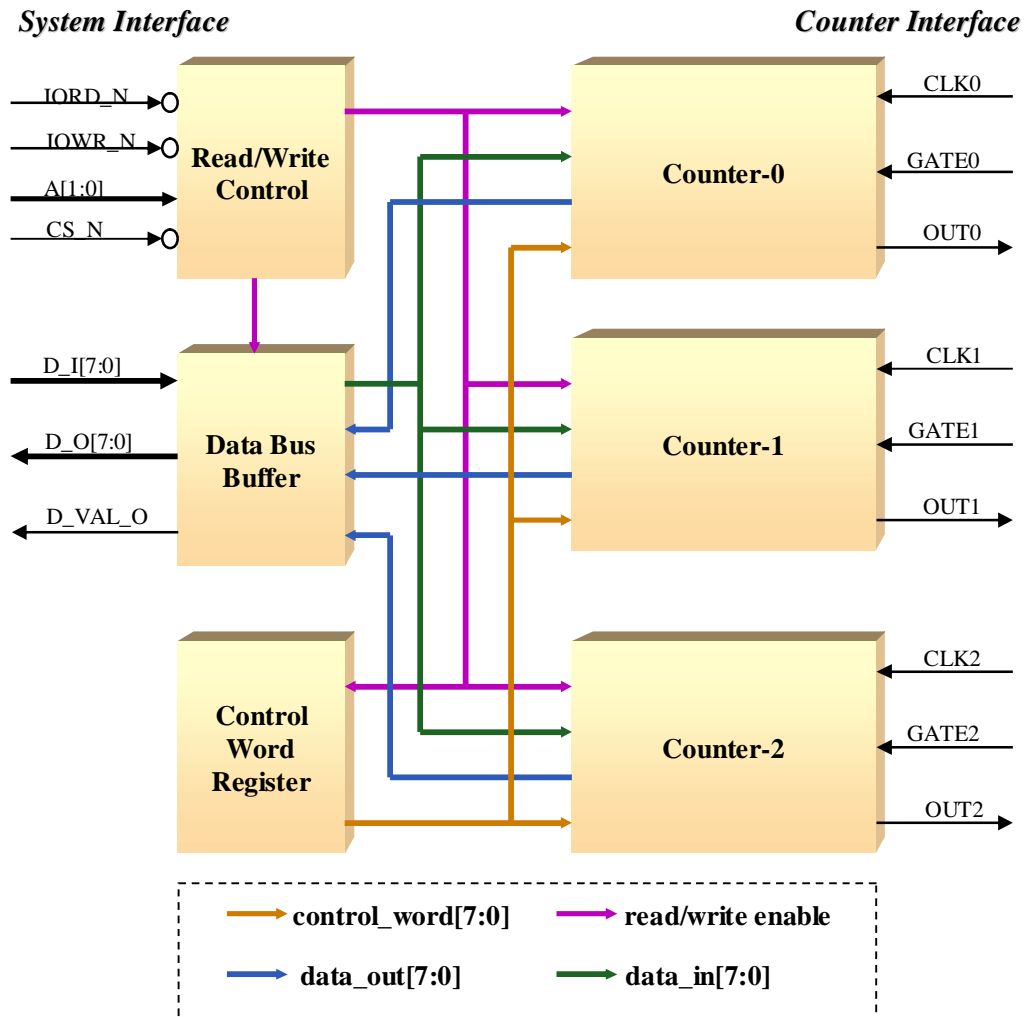
## 1.3 Acronyms and Abbreviations

**Table 1: Acronyms & Abbreviations**

Term	Meaning
BCD	Binary Coded Decimal

## 2 Programmable Interval Timer

### 2.1 Block Diagram



**Figure 1: Programmable Interval Timer Block Diagram**

### 2.2 Description

The design implements 8254 Programmable Interval Timer/Counter used for timing control applications in microcomputer systems.

Design is capable of generating accurate time delays under software control. Three independent 16-bit counters are supported which can be configured to operate in one of the six operating modes supported.

- **Data Bus Buffer:** This is a 8-bit, three-state buffer that interfaces the system bus to the remaining blocks of the design.
- **Read/Write Control:** This block decodes the control and address inputs from the processor and generates control signals to the remaining blocks of the design.
- **Control Word Register:** This is a 8-bit register into which the control words are written to determine the operation mode of the counter.
- **Counter #n (n=0, 1, 2):** Three independent counters capable of binary or BCD operation are supported. Each counter supports six different modes configurable through software and can each be set to different operating modes.



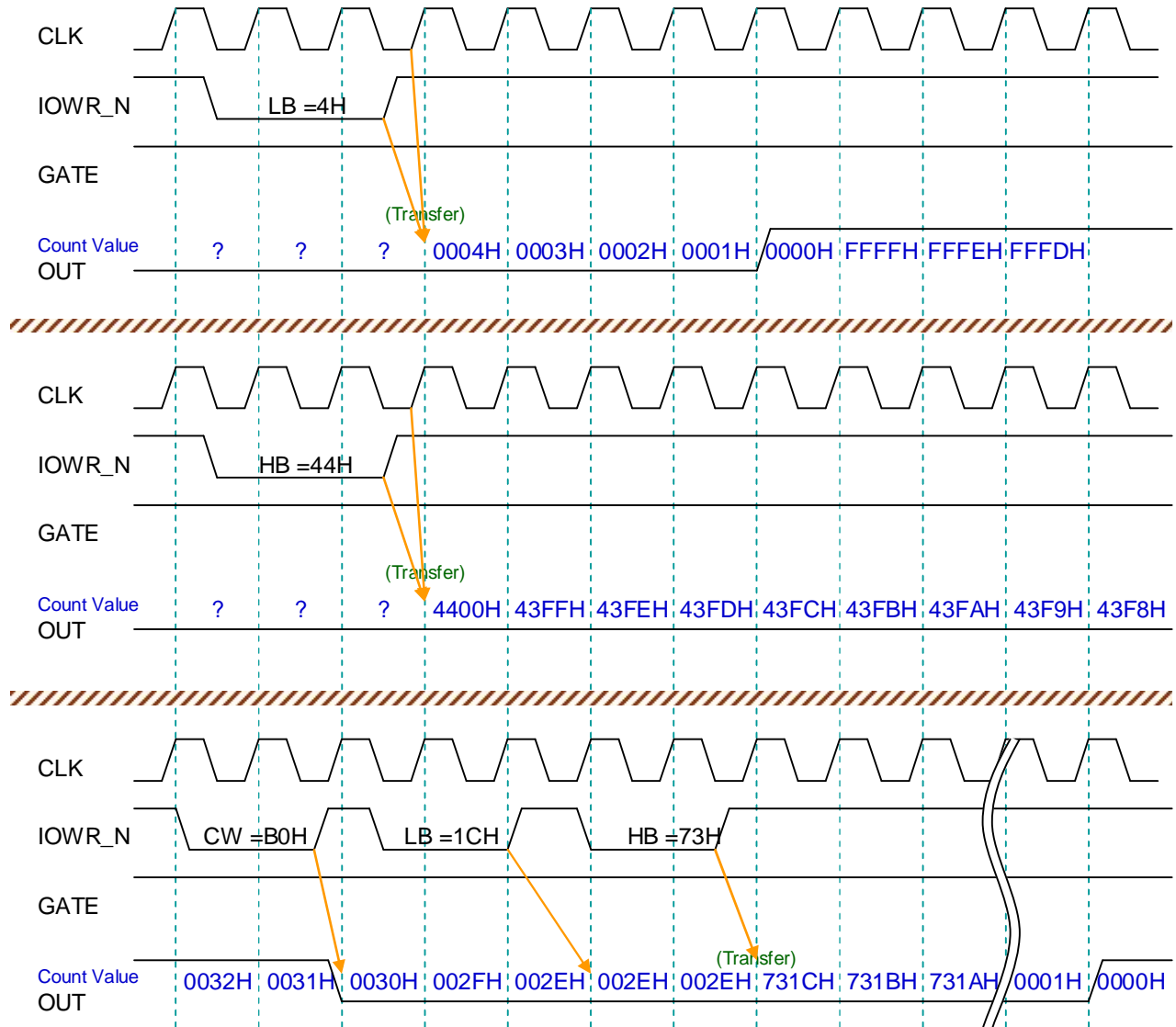
## 2.3 Signal Description

**Table 2: Programmable Timer IO Signal description**

SIGNAL NAME	I/O	WIDTH	DESCRIPTION
RESET	I	1	Input reset signal
D_I [7:0]	I	8	8-bit input data bus
D_O [7 :0]	O	8	8 bit output data bus
D_VAL_O	O	1	Output data valid signal
A [1 :0]	I	2	16-bit bidirectional data lines
CS_N	I	1	Active low Chip select input
IOWR_N	I	1	Active low Write enable input
IORD_N	I	1	Active low Read enable input
CLK0	I	1	Determines the count rate for Counter-0
GATE0	I	1	This signal controls the operation of Counter-0 depending on the mode of operation
OUT0	O	1	Counter-0 output, operation depends on the count mode. Can be used as an interrupt source for the processor.
CLK1	I	1	Determines the count rate for Counter-1
GATE1	I	1	This signal controls the operation of Counter-1 depending on the mode of operation
OUT1	O	1	Counter-1 output, operation depends on the count mode. Can be used as an interrupt source for the processor.
CLK2	I	1	Determines the count rate for Counter-2
GATE2	I	1	This signal controls the operation of Counter-2 depending on the mode of operation
OUT2	O	1	Counter-2 output, operation depends on the count mode. Can be used as an interrupt source for the processor.

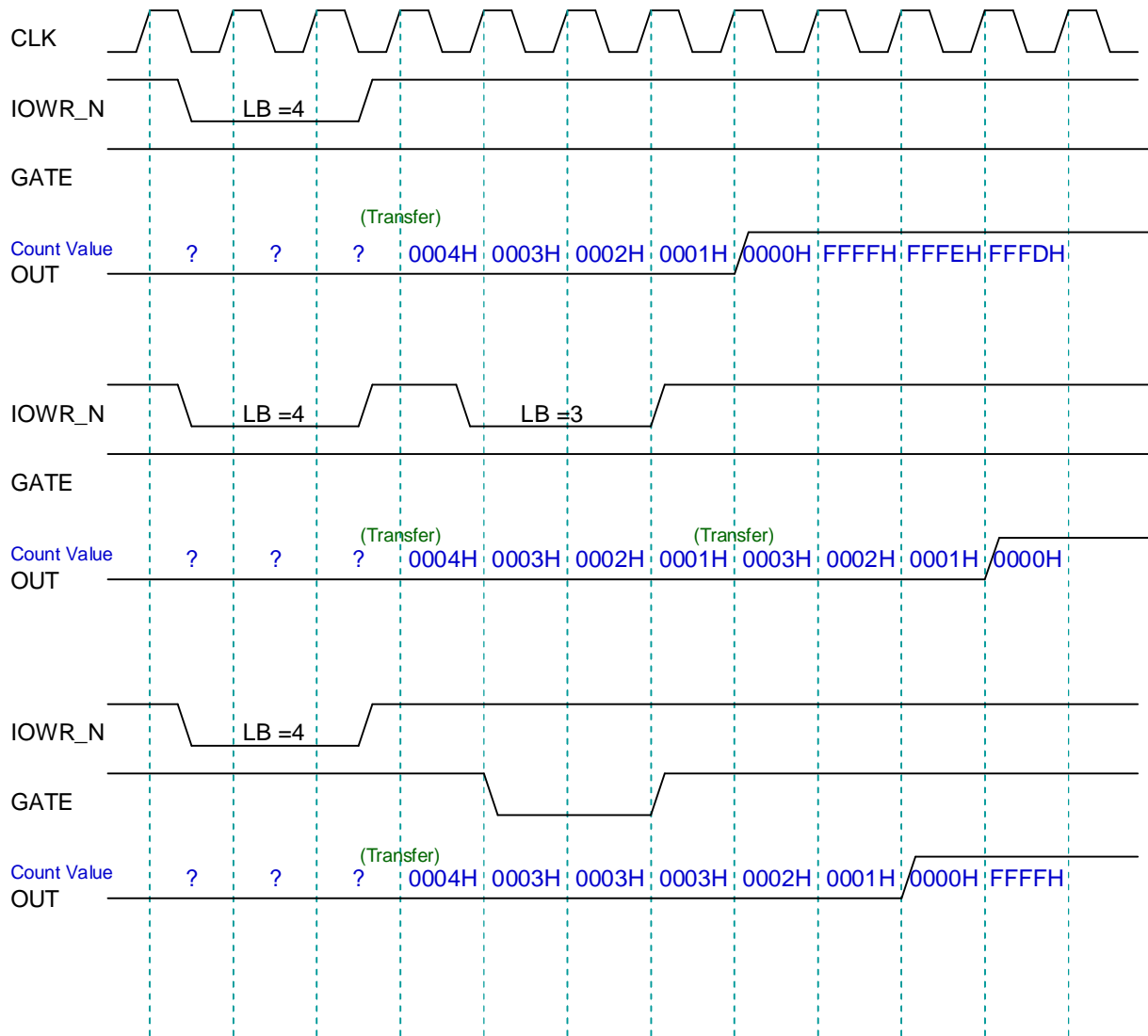
### 3 Timing Waveforms

#### 3.1 Count Write Operation (Ex. Mode 0)



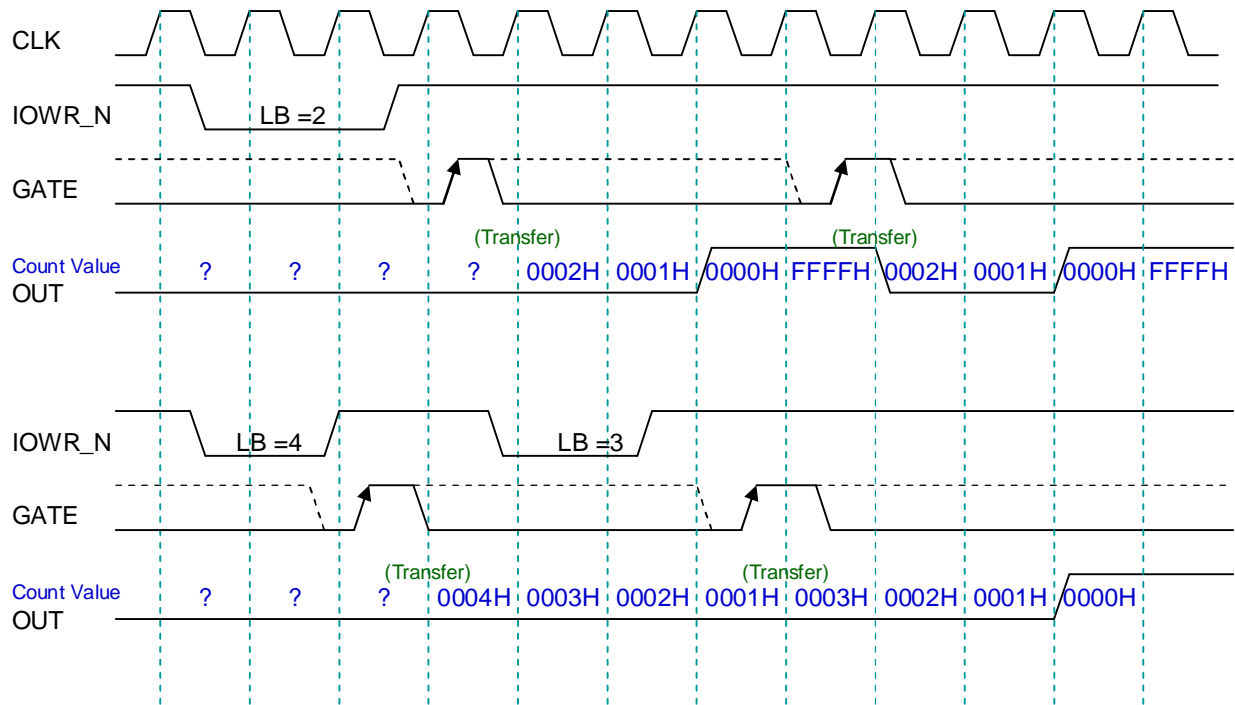
**Figure 2: Mode 0 Operation**

### 3.2 Mode 0 Operation



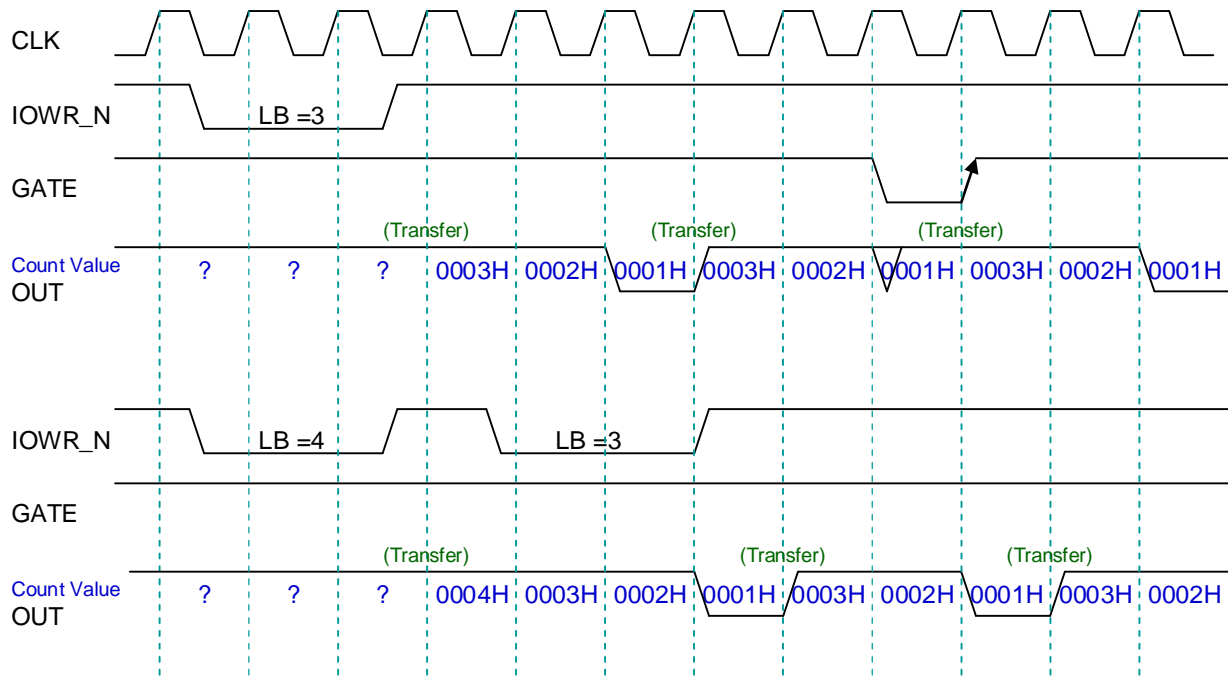
**Figure 3: Mode 0 Operation**

### 3.3 Mode 1 Operation



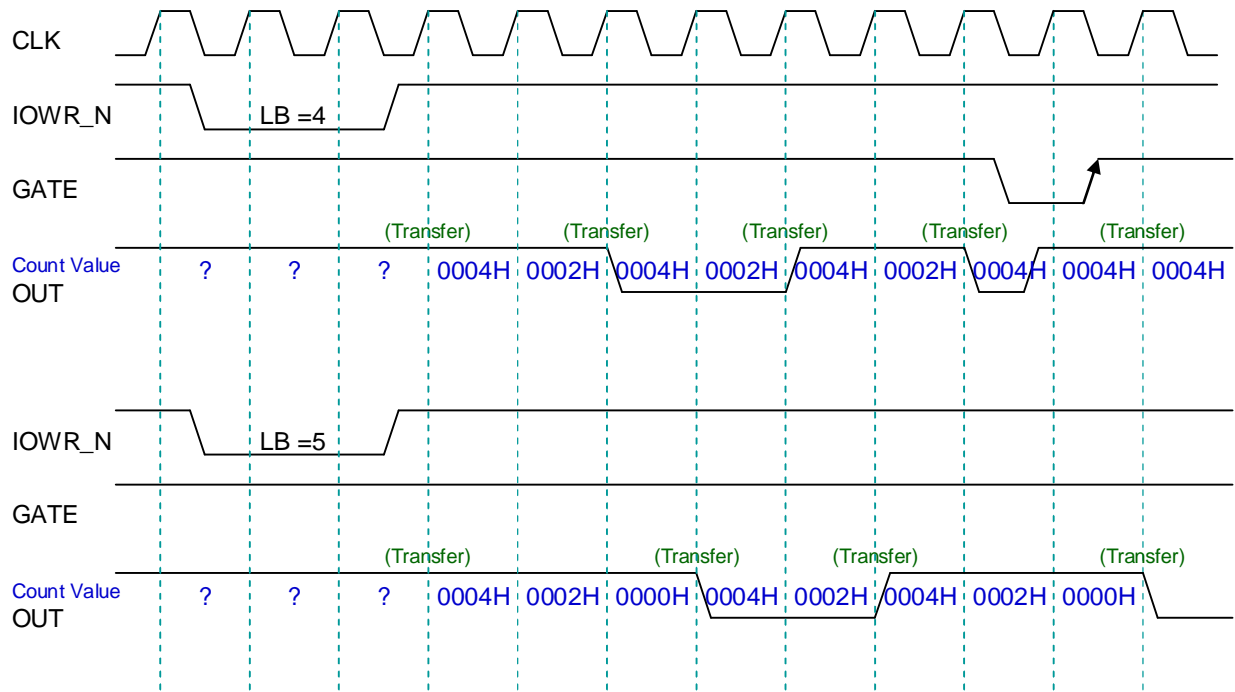
**Figure 4: Mode 1 Operation**

### 3.4 Mode 2 Operation



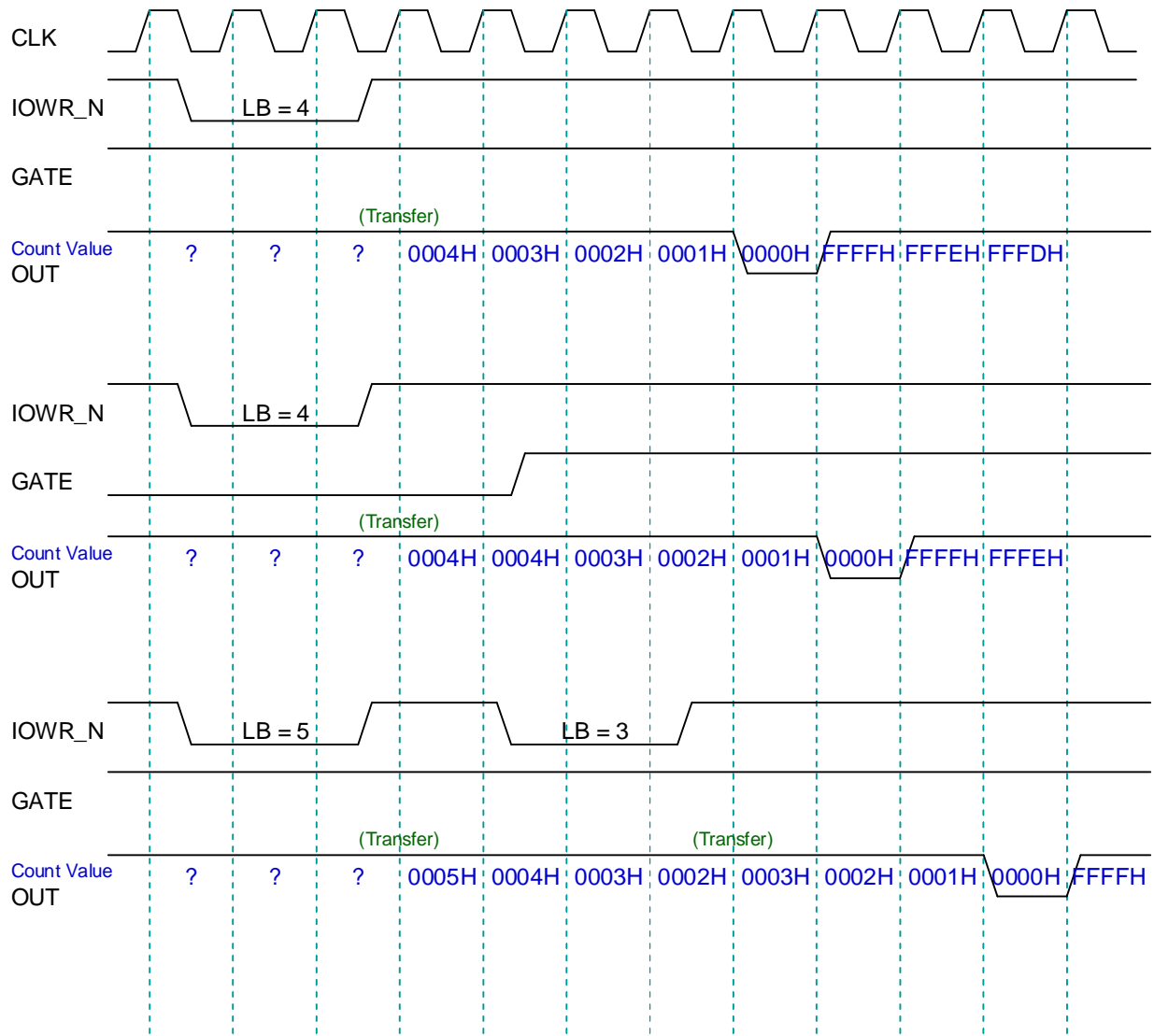
**Figure 5: Mode 2 Operation**

### 3.5 Mode 3 Operation



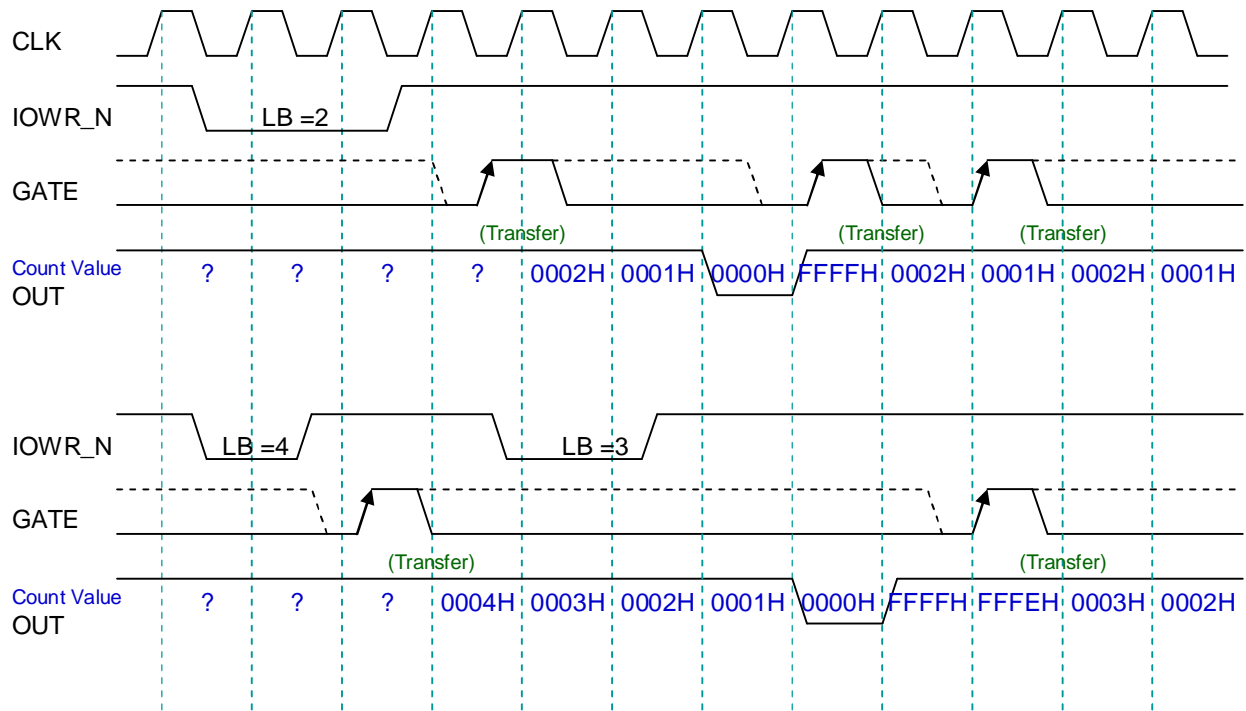
**Figure 6: Mode 3 Operation**

### 3.6 Mode 4 Operation



**Figure 7: Mode 4 Operation**

### 3.7 Mode 5 Operation



**Figure 8: Mode 5 Operation**