

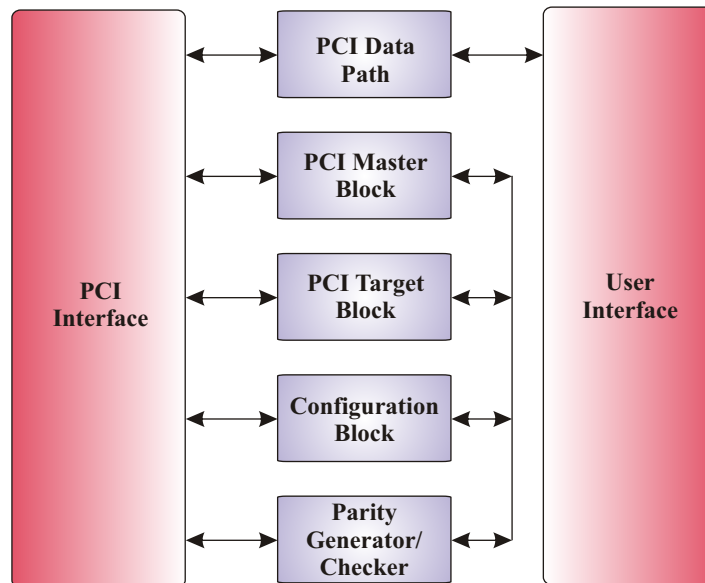
Overview

iW-PCI Controller provides an interface between the PCI bus and user interface. The core consists of PCI master block, PCI target block, Parity generator/Checker and etc.

Features

- ✧ 64-bit, 66MHz PCI interface
- ✧ Separate initiator and target functional blocks
- ✧ Supported initiator commands and functions:
 - ❖ Configuration read / write
 - ❖ Memory read / write, memory read multiple, memory read line
 - ❖ I/O read / write
 - ❖ Interrupt acknowledge, special cycles
 - ❖ Parity generation, parity error detection
 - ❖ Master abort
- ✧ Supported Target commands and functions:
 - ❖ Type 0 configuration space header
 - ❖ Up to six base address registers
 - ❖ Memory read / write, memory read multiple, memory read line
 - ❖ I/O read / write
 - ❖ Medium speed DEVSEL timing
 - ❖ Interrupt acknowledge
 - ❖ Parity generation, parity error detection
 - ❖ Target abort, target retry, target disconnect
- ✧ Supports a very generic user interface

Block Diagram



Deliverables

- ✧ Technical Specification
- ✧ RTL Verilog Synthesizable Code
- ✧ Comprehensive Test Environment
- ✧ Technical Support and Maintenance

About Us

iWave Systems Technologies is an embedded Hardware and Software Turnkey Design Services company, focused on providing integrated solutions for developing innovative products and systems in the areas of Communication, Consumer electronics and Multimedia. iWave offers complete turnkey solutions for systems engineering and product development.

Contact Us

India: iWave Systems Technologies Pvt. Ltd., 7/B, 29th Main, BTM Layout 2nd Stage, Bangalore 560 076. INDIA

Ph : +91-80-26683700, 26786245, Fax : +91-80-26685200

Email : mktg@iwavesystems.com, Web : www.iwavesystems.com

Japan: iWave Japan, Inc. 8F Kannai Sumiyoshi Building 3-29, Sumiyoshi-cho, Naka-ku, Yokohama Kanagawa, Japan.

Ph : +81-45-227-7626, Fax : +81-45-227-7646, Email : info@iwavejapan.co.jp, Web : www.iwavejapan.co.jp

Note : iWave reserves the right to change these specifications without notice as part of iWave's continuous effort to meet the best of breed specification.
The registered trade marks are properties of their respective owners.

Supply of this core does not convey nor imply a right under the patent rights of the respective patent holders, if any, to make use or sell any product employing these patent rights.
A patent license from respective patent holder may be required for any use of such patent rights, including the implementation of the core in an FPGA or an Integrated Circuit or any other device.