iW-PCIe to ISA Bridge

Introduction

The iW-PCIe to ISA Bridge consists of a single ISA bus controller & a Xilinx endpoint core for PCIe with PHY interface. The PCIe bridge is a 32 bit PCI express interface that fits into a single Spartan3 FPGA.

Features

PCIe Interface :

- 32 bit PCIe interface with Xilinx endpoint core for PCIe with external PHY hardware.
- The Xilinx endpoint core for PCIe follows PCI express base specification v1.1 layering model
- Endpoint core implements the physical layer, datalink layer, transaction layer & configuration management layer
- Six individually programmable BAR's & expansion ROM BAR
- MSI & INTX emulation.
- Removal of corrupt packets for error detection and recovery
- Compatible with PCI/PCI Express power management functions
- Used in conjunction with NXP PX1011A PCI Express standalone PHY to achieve high transceiver capability
- 2.5 Gbps line speed, Automatic clock and data recovery, 8b/10b encode and decode
- Maximum transaction payload of up to 512 bytes

ISA Interface :

- The ISA bridge implements a 16 bit data interface
- Bus clock of 6 to 8Mhz for ISA interface
- 20 bit system address lines tristate which can be latched on to the falling edge of bus address latch enable signal
- Latchable address lines, these unlatched address signals give the system up to 16 MB of address ability

Description

The PCIe Bridge has an endpoint PIPE v1.7 (PHY Interface) for PCIe 1 lane core from Xilinx, Programmed I/O module & ISA bus controller. The endpoint core from xilinx implements the physical layer (PHY interface), data link layer, transaction layer & configuration management layer of PCIe base specification v1.1 layering model. A external PCIe PHY device is needed in the PHY Interface side to complete the 1 lane PCIe link.The PIO design interfaces with the endpoint for PCI Express core's transaction interface & responds with read/write transaction for memory or IO transaction from the endpoint core.

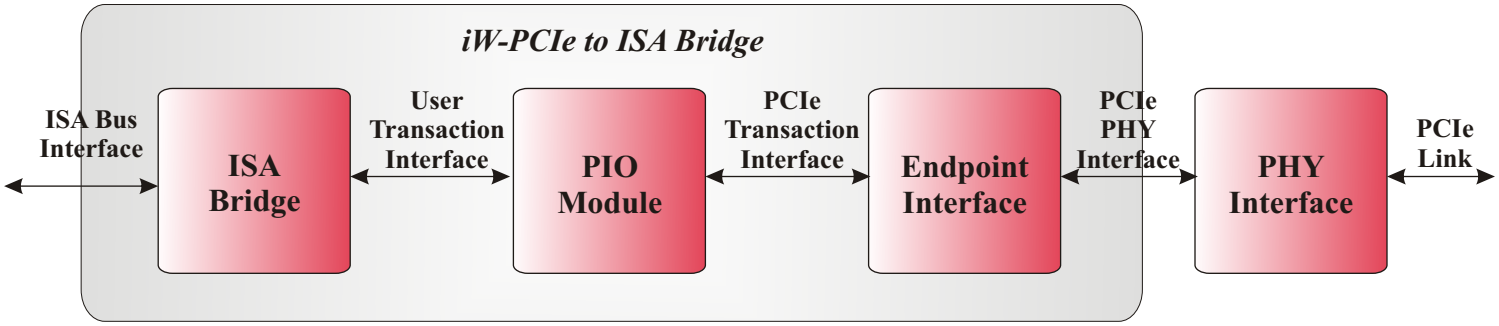
The ISA bridge is implemented in user interface side of the PIO design. The host processor can access the unit through I/O or memory read and write commands. The ISA bus is a 16bit interface which can be used to connect peripheral components to the host cpu through ISA bus. PCIe bridge supports the 32 bit data transfer between host cpu & peripheral components connected through ISA bus in ISA bridge side.

Example Application

The below diagram shows the example application for the PCIe to ISA bridge, which requires a additional PHY device to connect peripheral components to the host CPU using ISA bus.

The bridge requires a standalone PHY hardware to form a complete PCIe link. The PHY handles the low level PCI express protocols & signaling. The ISA bridge can be used to transfer data between the host CPU & computer peripherals which are connected through ISA bus.

Figure-1 : PCIe to ISA bridge Block Diagram & Example Application



Device Utilization Summary

IP	Xilinx Device	Fmax (MHz)	Slices	4 input LUTs	IOB	GCLK	BRAM	DCM	Power (mW)	Design Tool
PCIe ISA Bridge	XC3S700A	110	4,856 (82%)	6,911 (58%)	84 (27%)	4 (16%)	8 (40%)	1 (12%)	66	9.2.04i