

Overview

iW- 80186EB is a powerful 16 - bit microprocessor core, executes instruction list compatible with 80186EB microprocessor. The design along with multiple peripherals can be fit into single FPGA.

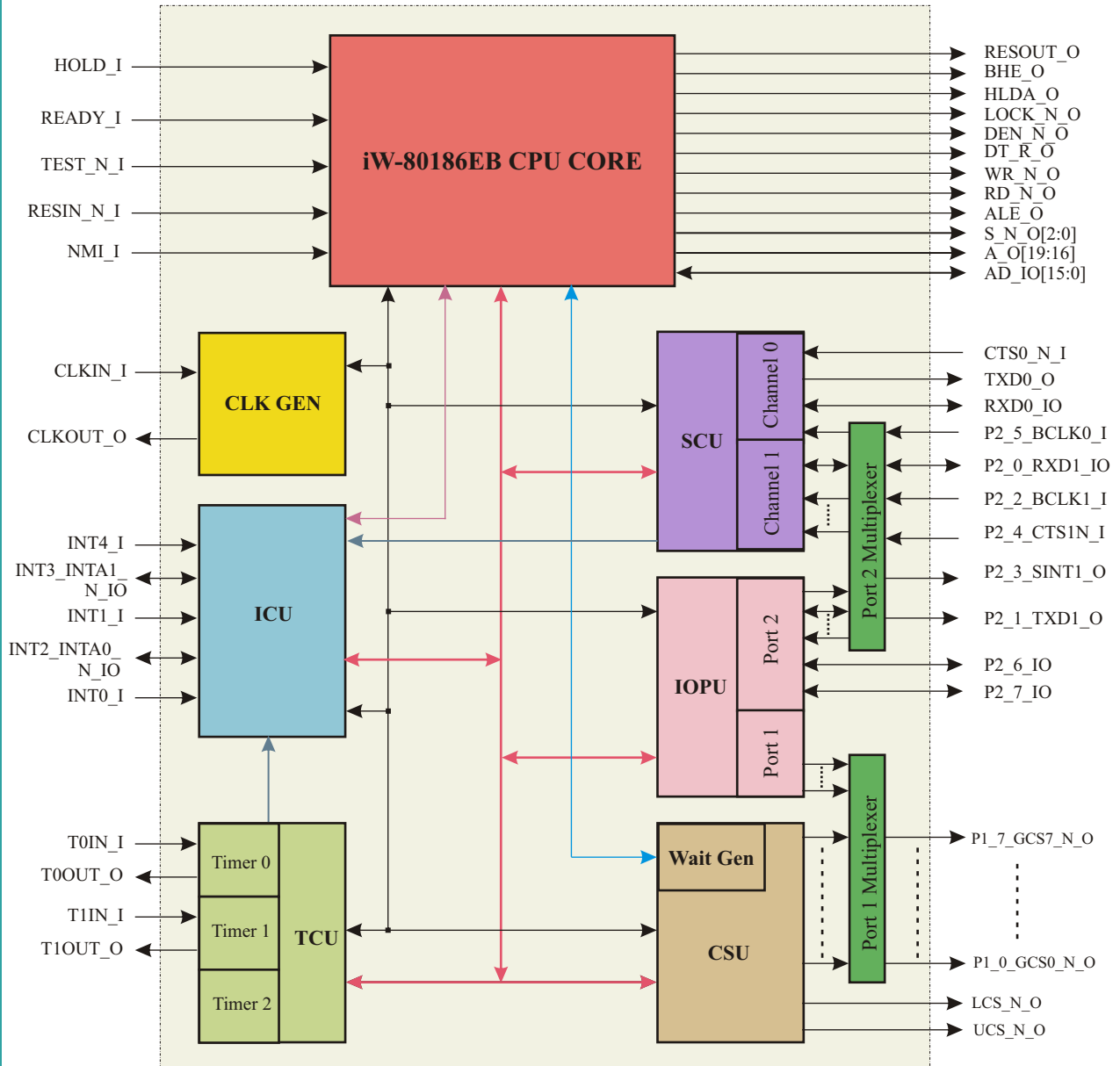
Features

- ❖ iW-80186EB Core
 - ✘ Multiplexed 20 - bit address and 16 - bit data bus
 - ✘ 1MB memory space divided into 4 segments
 - ✘ 64KB IO space
 - ✘ Non Maskable Interrupt support
 - ✘ Arithmetic - Logic Unit
 - # 8, 16 & 32 - bit operations
 - # 8 & 16 - bit logical operations
 - # Boolean manipulations
 - # 16 x 16 bit multiplication (signed or unsigned)
 - # 32/ 16 - bit division (signed or unsigned)
- ❖ CPU on - chip peripherals
 - ✘ Programmable Timer / Counter Unit
 - # 3 programmable independent 16 - timers
 - # TOUT0 to TOUT1 pin outputs
 - # TIN0 & TIN1 used either as clock or control signals
 - # Timer - 2 can be used to clock other 2 timers
 - # Internal / external input clock selectable
 - ✘ Serial Communication Unit
 - # RS - 232 - C protocol support (on - chip CTS_N, SINT_N pins)
 - # Both synchronous and asynchronous modes are supported
 - # Two independent identical channels
 - # Full duplex operation in asynchronous mode
 - # Half duplex operation in synchronous mode
 - # Programmable 7, 8 or 9 data bits asynchronous mode
 - # Independent baud rate generator
 - # Double buffered transmit and receive
 - # Clear - to - Send feature for transmission
 - # Break character transmission and detection
 - # Programmable even, odd or no priority
 - # Detects both framing and overrun errors
 - # Supports interrupt on transmit and receive
 - ✘ Interrupt Controller Unit
 - # Edge trigger / level trigger selectable
 - # Individually maskable interrupt requests
 - # Programmable interrupt request priority orders
 - # Supports cascading (only INTP0 and INTP4)
 - # 5 external interrupt request inputs (INTP0 to INTP4)
 - # 2 internal interrupt input pins (SCU and TCU)
 - ✘ Chip Select Unit
 - # Ten programmable chip - select outputs
 - # Programmable start and stop address
 - # Memory or I/O bus cycle decoder
 - # Programmable wait - state generator
 - # Provision to disable a chip select
 - # Provision to override bus ready
 - ✘ Clock Generator
 - ✘ Two 8 - bit multiplexed I / O ports

Core Benefits

- ❖ Compatible with Intel 80186EB instruction set
- ❖ High FPGA integration enables lower BOM cost and smaller board design
- ❖ Supports retarget and merge external peripherals and traditional custom old ASICs
- ❖ Enhancements of system performance with increased operating frequency and integration

Block Diagram



Core Applications

- ❖ Quick migration of 80186EB based designs to an FPGA platform
- ❖ Replacement for 80186EB processor and ASICs
- ❖ Typical processor applications such as industrial, automotive and etc.

Deliverables

- ❖ Technical Specification
- ❖ RTL Verilog Synthesizable Code
- ❖ Comprehensive Test Environment
- ❖ Technical Support and Maintenance

About Us

iWave Systems Technologies is an embedded Hardware and Software Turnkey Design Services focused on providing integrated solutions for developing innovative products and systems in the areas of Communication, Consumer Electronics and Multimedia. **iWave** offers complete turnkey solutions for systems engineering and product development.

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